Reply To Examiner's Remarks

Claims 1-15 are presented for consideration.

The Examiner rejects claims 1-15 under 35 U.S.C. 103(a) as obvious from the combined disclosures of U.S. Patent No. 6,301,596, issued to Karanovic, and U.S. Patent No. 4,727,506, issued to Fling. The Karanovic patent discloses, in Figures 1 and 4 and in columns 2 and 3, a partial sum filter system and method. The system forms an accumulated value signal value AV(n) at stage or time number n that is expressible mathematically as

$$AV(n) = C(n-1) \times IV(n-1) + RN(n-1) + AV(n-1), \quad (1)$$

C(n-1) = filter coefficient value at time n-1,

IV(n-1) = input signal value at time n-1,

RN(n-1) = random number generator value at time n-1,

AV(n-1) = accumulated signal value at time n-1.

Only the K most significant bits (MSBs) for the right hand quantity in Eq. (1) are kept. The dithering is driven by the bit or bits supplied by the random number generator 30 in Figure 1 of the Karanovic patent (column 2, lines 18-20 and 50-53).

The Examiner asserts that the Fling patent discloses, in connection with Figure 5 of that patent, use of an EXclusive OR (XOR) operation to provide a varying or random signal value V(n) in place of a signal value dithering operation used in Figure 2 or 3 of the Fling patent, where V((n) appears to be computed as

$$V(n) = OV(n-1;72) \otimes \ldots \otimes O(n-1;75) \otimes OV(n-1;76), \quad (2)$$

OV(n-1;k) = output value of gate k at time n-1 in Figure 5.

Accepting without deciding that this assertion is valid, when the random number value RN(n-1) in Eq. (1) is replaced, Eq. (1) is re-expressed as

$$AV(n) = C(n-1) \times IV(n-1) + \{OV(n-1;72) \otimes \ldots \otimes OV(n-1;75) \otimes OV(n-1;76)\} + AV(n-1), \quad (3)$$

where a bit value OV(n-1;k) (k = 72, ...,76) is identified with one of the accumulated signal AV bit values at a preceding time.

Claim 1 of the subject patent application recites a method for adjusting a low frequency noise floor for a filtered signal, where the method comprises:

providing a digital signal, having M bits, that has been digitally filtered, where M is a selected positive number;

forming an EXclusive OR product of N LSB bits of the M-bit filtered signal, to provide a one-bit supplement signal, where N is a selected positive number satisfying $N+1 \leq M$;

adding the supplement signal to the M-bit filtered signal to produce a modified filtered signal; and

removing L LSB bits from the modified filtered signal to produce a dithered, filtered signal, where L is a selected positive number satisfying $L+1 \leq M$.

With reference to Figures 1 and 2 of the subject patent application, and adopting the notation used in Eq. (1), claim 1 can be expressed mathematically as

$$AV(n) = S1(n) = C(n-1) \times IV(n-1)$$
$$+ \{AV(n-1;1) \otimes AV(n-1;2) \otimes ... \otimes AV(n-1;N-1) \otimes AV(n-1;N)\}, \quad (4)$$

where AV(n-1;k) is the kth bit of the accumulated value signal AV(n-1) and the bracketed term in the second line of Eq. (4) is an EXclusive OR product of the N bits of the accumulated value signal AV(n-1).

Comparing Eqs. (3) and (4), one notes that the first term, C(n-1) x IV(n-1), is the same for each of these expressions. The remaining additive quantities in Eq. (3) are

$$\{OV(n-1;72) \otimes ... \otimes OV(n-1;75) \otimes OV(n-1;76)\} + AV(n-1),$$

where OV(n-1;k) is identified with a bit value of the accumulated value AV(n-1). By contrast, the remaining additive quantity in Eq. (4) is expressible as

$$\{AV(n-1;1) \otimes AV(n-1;2) \otimes ... \otimes AV(n-1;N-1) \otimes AV(n-1;N)\}.$$

These remaining quantities from Eq. (3) and from Eq. (4) are clearly different and are not generally equivalent to each other. The remaining quantity from Eq. (3) includes the additive term AV(n-1) plus a truncated EXclusive OR product involving the bit values AV(n-1;k) (k = 72, ... , 76). The remaining quantity from Eq. (4) involves a single EXclusive OR product

$$\{AV(n-1;1) \otimes AV(n-1;2) \otimes ... \otimes AV(n-1;N-1) \otimes AV(n-1;N)\}$$

and no further additive term AV(n-1), as in Eq. (3).

Because of these differences, including the presence of additional terms in Eq. (3) with no equivalent counterpart in Eq. (4), the right hand side of Eq.(3) is not the same as, and is not generally equivalent to, the right hand side of Eq. (4). For these reasons, the Applicant believes that method claim 1 from the subject patent application is not made obvious from the combined disclosures of the Karanovic patent and the Fling patent. The independent system claim 6 and the independent article of manufacture claim 11 are parallel to independent claim 1 and are believed to be allowable for the same reasons that claim 1 is allowable. Claims 2-5, 7-10 and 12-15 depend upon the respective claims 1, 6 and 11 and are believed to be allowable if the corresponding claim 1, 6 and/or 11 is allowable.

The Applicant requests that the Examiner pass the application, including claims 1-15, to issue as a U.S. patent.

Respectfully Submitted,

John Schipper

Date: 06 June 2003

John Schipper

Patent representative for Applicant